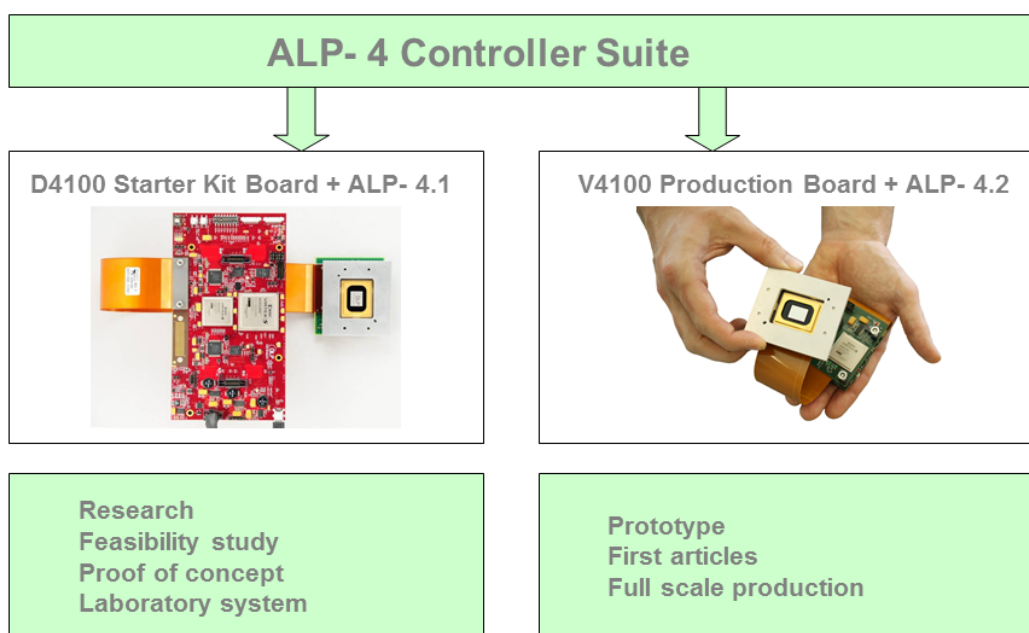


# ALP-4 Controller Suite

## for DLP® Discovery™ 4100 Chipsets

The ALP Controller Suite, developed and produced by ViALUX, gives the user access to the full performance of the DLP® Discovery™ chipsets without the need of time consuming developments for hardware, firmware and high-frequency FPGA logic code.

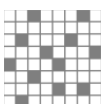
ALP Controllers offer flexible tools for programming DLP® operations from PC and they are available for both, DLP® Starter Kit Boards and DLP® Serial Production Boards. The customer can migrate from the Starter Kit environment to the V4100 ViALUX production platform without any additional programming efforts.



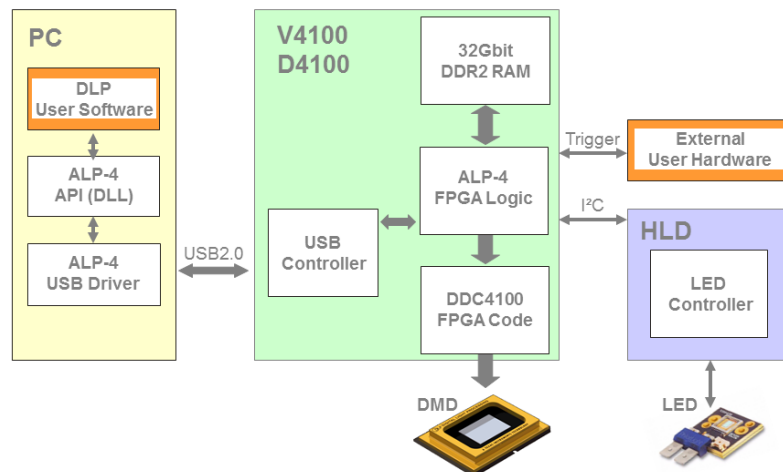
The outstanding switching speed of the DLP® Discovery™ DMD is supported to its full extend enabling 22 727 XGA full array switches per second. The user can operate with binary and gray value patterns, respectively.

The ALP Controller Suite implements a fast and reliable USB2.0 PC interface with enhanced effective transfer rate by lossless on-the-flight compression of data. Data rates up to 1.2 Gbit/s are achieved that corresponds to 1 600 XGA frames per second. The ALP-4 driver is robust, validated, UIF compliant and well suited for industrial use. Microsoft Windows operating systems are supported up to Windows 7 both, x32 and x64.

ALP Controllers support all DMD formats of the DLP® Discovery™ Starter Kit Boards of all platforms and, in particular the most powerful current Discovery™ 4100 systems. A well organized and easy to use application programming interface (API) is provided for programming the DLP® System conveniently. The API library (DLL) is portable and can be used in C++, VBasic, .NET, LabView, and MATLAB. Multiple USB ALP devices may run at the same time and they can be controlled from the same application program. ALP Controllers are upwards compatible enabling smooth migration to the next higher platform.



## Principle of operation



Sequences of patterns are generated in the PC and uploaded to the on-board memory (32 Gbit SDRAM) via compressed USB2.0 transfer. Optimized FPGA logic code guarantees precise, triggered transfer of SDRAM data to the DMD array with 24 Gbit/s data rate. An Image Scrolling option has been added for all cases where the projection is aiming at a moving screen (substrate) as it is typical in all types of direct imaging.

The ALP Controller provides high flexibility by free choice of properties of the sequence (bit depth, picture time, trigger control, repetitions). In this way, the pattern sequences can be customized to meet the respective application requirements.

An additional I<sup>2</sup>C interface is implemented to control and monitor LED light sources in connection with the DMD operation. The ViALUX HLD high-power LED driver is addressed via the ALP-4 application programming interface. It allows to adjust the brightness and to read the LED junction temperature for thermal management.

ViALUX offers two ALP-4 models, high-speed and basic. The high-speed controller enables maximum switching rates under full-array global shutter operation, gray value patterns and precise triggering while the basic model provides the full flexibility of single line operations. The specification for both models are given in the table below.

### ALP-4 high-speed

		0.7 XGA DMD		0.95 1080p DMD	
DMD area updated	# of Bits	# of lines	switching rate	# of lines	switching rate
full array	1 – binary	768	22 727 Hz	1 080	10 638 Hz
full array	6 – gray	768	1 092 Hz	1 080	845 Hz
full array	7 – gray	768	569 Hz	1 080	476 Hz
full array	8 – gray	768	291 Hz	1 080	255 Hz

### ALP-4 basic

		0.7 XGA DMD		0.95 1080p DMD	
DMD area updated	# of Bits	# of lines	switching rate	# of lines	switching rate
full array	1 – binary	768	300 Hz	1 080	100 Hz
single line	1 – binary	1	2 000 Hz	1	2 000 Hz

